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A Dual-Loop PLL with DAC offset for Frequency Shift While Maintaining Input Tracking

Abstract

A phase-locked loop (PLL) keeps tracking a reference clock when a frequency offset is introduced. The PLL has primary and secondary PLL loops. A digital-to-analog converter (DAC) generates a current that is passed through an offset resistor to generate an offset voltage. An op amp is inserted in the primary loop between a filter capacitor and a voltage-controlled oscillator (VCO). The offset resistor is coupled between the inverting input of the op amp and the op amp's output. When the DAC offset occurs, the voltage to the VCO and the frequency of the primary loop change and the primary loop loses tracking of the reference clock. The secondary loop keeps tracking the reference clock during the DAC offset while the primary loop is open. Then the output clock of the secondary loop is applied as the feedback clock to the phase comparator of the primary loop.